Digital Current Control of Electric Arc Furnace by Parallel Modular Three-Phase IGBT Inverters

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***Abstract*— Electric Arc Furnaces (EAF) have been traditionally fed by means of a medium- to low-voltage transformer (between grid and electrodes), where the main control action consists of modifying the electrodes vertical position. This simple and robust arrangement suffers from grid "pollution" and poor current control. Current control of EAF by means of three phase modular inverters is reported here for the first time. Several control issues are analyzed and addressed, ranging from pure control (e.g. addressing load imbalance and limits due to low switching frequency) to system management. Two different current regulation methods are proposed and compared, namely a scalar approach and a vector method using "quasi-zero phase-lag" sampling and gains adaptation. The second technique achieves very good control, leading to lower oversizing of the converter stage and process optimization. Simulations have been performed including digital controller architecture, converters and arc electrical behavior. Preliminary experimental measurements are reported based on an actual plant.**

Keywords — Electric Arc Furnace, inverter, paralleled inverter, adaptive current control.

I. INTRODUCTION

The purpose of the EAF power system is to transfer heat to the metallic material in the furnace, by igniting electric arc conduction between graphite electrodes and the material to be heated. In fact, the electric arc corresponds to a high temperature plasma region, from which heat is propagated to the surrounding. Control of three-phase Electric Arc Furnaces has been traditionally accomplished by changing the electrodes vertical position (by means of hydraulic actuators), which ultimately modifies the arc length (distance between electrode tip and conducting material inside the furnace). A step-down transformer is normally adopted for feeding the electrodes, usually characterized by significant series impedance, which helps arc stability, provides current limitation and mitigates grid current harmonics. This solution is very robust, but suffers from several issues, especially the "pollution" of the electrical grid [1] (e.g. flicker, harmonics) and low Power Factor (PF), which require oversizing the power distribution system. Moreover, controllability is poor, since the mechanical system dynamics (hydraulic actuators) is slow compared to the quickly changes of electric arc conduction. In fact, the arc current vs. voltage behavior is complex and nonlinear, [2]-[4], especially in the initial phase of the process.

Introducing power electronic conversion with fast current regulation represents a benefit for the entire process, guaranteeing reliable operation of the EAF close to its full heating capability, together with grid harmonics reduction and PF increase. Savings in materials (e.g. electrodes), energy and processing time are also expected, improving productivity. However, direct control of the arc current by means of power electronics was not feasible until very recent times, since the nominal power of a typical EAF is typically up to some tens of MW. Recent attempts at the introduction of controlled power converters in this application field are based on Active Series Reactor (ASR), allowing to dynamically change the impedance value during steel production process, [5]. Although this represents an interesting improvement over the typical EAF, controllability remains limited.

In this paper, current control of EAFs by means of three-phase modular inverters (Insulated Gate Bipolar Transistor based) is introduced for the first time. Several theoretical and practical control issues related to EAF application are analyzed and addressed. The different conditions which occur during the process, such as strong load imbalance, open-circuit, (i.e. "two-electrodes" or "single-phase" operation) and short-circuit, are efficiently and safely managed. Two different current control methods are proposed and compared in simulation, one of them considering the 3-phase current and voltage RMS values ("scalar" control) and the other applying instant current control in the stationary reference frame ("vector" control). It will be shown that, despite the scalar control can lead to acceptable behavior, vector control obtains superior performances, with very stable RMS current level and fast current limitation. This is made possible by addressing specific details, such as time-varying load behavior, low switching frequency and large latency of the distributed control architecture. Adaptation of current controllers based on real-time estimation of load impedance and "quasi-zero phase-lag control" represent original solutions to these problems, aiming at maximization of the current regulation bandwidth, which allows lower oversizing of the power converter stage, finally resulting in cost reduction.

Simulation investigation, optimization and validation prior to implementation of control algorithms have been performed by reproducing the overall digital control architecture and power electronic converters, including communication constraints among different modules and controllers. Both a complete analytical model from literature on gas discharge [1], and a novel empirical one, based on measurements from an actual plant, have been used for modeling the arc voltage/current relation. Finally, experimental results will be presented for an actual EAF plant. The most important

simulation results and preliminary experiments are presented, in order to validate the proposed concepts.

II. System Architecture

A sketch of the system architecture of the EAF application based on static power converters is shown in Fig. 1. On the left two parallel three-phase inverter modules are connected to a common distribution network. The furnace is placed beyond the wall, including electrodes and hydraulic actuators for vertical movement. The converter is composed by two three-phase inverters in parallel, coupled by series inductors. IGBT switching frequency is 1 kHz, but control update is performed with double-update PWM [6]. A control strategy, similar to the one in [7], has been developed to address the additional degree of freedom due to the parallel topology. In fact, even if the same switching commands are applied, the two currents might be different due to physical path or driving imbalance. Moreover, different current setpoints could be set, e.g. for fault-tolerance or temperature balancing. Details about this and the inverter hardware are reported in Table I.

III. Current Control Issues

The EAF supply converter is a peculiar case in terms of output requirements. The electric arc load is in fact strongly non-linear and variable, which also results in heavy imbalance. Given that switching frequency is very low, current control cannot be reasonably expected to obtain low harmonic distortion. Conduction behavior at each electrode tip is subjected to fact fast variations (especially at the beginning of the process), due to sudden motion of the solid metal.

Moreover, due to the unknown plant characteristics, non-linearity and imbalance, most traditional control techniques, such as synchronous current control, are ineffective or not applicable. It should also be considered that the electrode height control (via hydraulic actuators) is also performing a control action, which has the main purpose of igniting or restoring the arc and obtaining the optimal arc characteristics. This also complicates current control, since every mechanical variation introduces disturbance to the electrical system and ultimately to current control.

On the other hand, accurate regulation (e.g. low harmonic distortion) is not a crucial aspect within the production process, since the main purpose is generating heat within the furnace. The controller is then expected to properly manage heat generation within the furnace. In terms of current control, this means that the objectives are slightly different than usual cases, i.e. the following objectives are pursued:

- accurate regulation of the RMS current value (i.e. thermal transfer is ensured, despite current distortion);
- fast and effective current limitation, in order to minimize the oversizing of the power converter stage;
- maximization of the conduction time (i.e. minimizing the occurrence of arc shut-off events) on all phases, compatibly with boundary conditions.

Since the behavior of the arc discharge is passive, a simplified model can be built for the first-harmonic only, where each arc conducting channel is represented by a variable resistance.

The overall equivalent circuit seen by the inverter is a resistor-inductor model, with strongly variable resistance. Considering the three wye-connected impedances at the inverter output, this translates into two main consequences:

- the star center voltage is unknown (since it strongly depends on the load imbalance);
- the equivalent impedance on a rotating axis (i.e. synchronous frame) varies within the electrical period.

In particular, the second characteristic makes synchronous reference frame current control not practical, especially regarding stability (positive-negative sequence reference frame [8] are not suitable as well). The two proposed current control methods will be presented hereafter. In both cases, tuning criteria have been developed, and gain adaptation based on estimated impedance has been adopted.

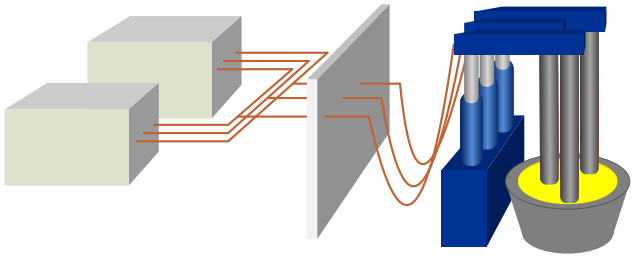

Fig. 1. Schematic view of the inverter and EAF layout (two parallel converters) and actual EAF picture.

A. *Load management: open-circuit, partial open-circuit and short-circuit*

The proposed control schemes provide current regulation in normal operating conditions, i.e. when arc is ON (i.e. ignited) on all the three electrodes, while the situations in which arc is shut-down (i.e. open-circuit) on one or more phases need to be considered separately. The operation modes can be resumed as follows:

- Conduction (i.e. arc ignited) on all three phases (“3ON”);
- Three phases open-circuit (“3OFF”);
- One phase open-circuit, i.e. arc ignited on two phases (“1OFF”);
- Short-Circuit on one or more phases (“SC”).

The first step towards the implementation of a management strategy is the on-line determination of the actual operating mode, so that proper action can follow the detection of any mode change. The aim is to provide the most stable and smooth operation possible, which minimizes the occurrence of fault conditions and eventually maximizes on-time and productivity of the EAF plant. While short-circuit on a certain phase is easily detected when instant absolute value of current is above a certain limit, the other conditions pose some

challenges. In fact, avoiding false recognition of 3OFF or 1OFF is important for guaranteeing the best possible continuity of operation.

The criteria adopted for detecting the various modes are based on real-time estimation of the phase impedance (scalar magnitude value). The definition of phase impedance, as adopted for the purpose of arc conduction detection, is based on the "fast-RMS" values (as will be defined in paragraph III.B) of phase voltage and current:

$$\hat{Z}_{a,b,c} = \frac{V_{RMS_{a,b,c}}}{I_{RMS_{a,b,c}}} \tag{1}$$

If the estimated value overcomes a "high" threshold, "open-circuit" is detected on the considered phase, while a value lower than the "low" threshold corresponds to entering the normal conduction mode. The changeover between operating modes is ruled by an hysteresis logic as shown in Fig. 2. Open-circuit is assumed at the algorithm startup. The two thresholds are calculated based on the nominal resistance value, i.e. the ratio

$$R_{nom} = \frac{V_{nom}}{I_{nom}} \tag{2}$$

Short-circuit is a condition in which, in principle, current could be controlled by the normal regulator (thanks to the presence of series inductance). However, since the change from high arc voltage to short-circuit could happen abruptly (especially in the early stages of the heating process), fast current limitation should occur before the intervention of hardware protections on IGBT modules. Current limiting is obtained by applying a bang-bang controller only when current threshold is overcome. Current thresholds are chosen based on the maximum peak current acceptable, while voltage hysteresis values are determined based on the maximum current swing in one period (given inductance) and considering the worst-case (i.e. short-circuit).

Operation in 1OFF mode must be considered separately because, differently from 3ON, only one "degree of freedom" (i.e. independent circuit variables) is present. In fact, the equivalent circuit only consists of two output phases in series, which translates into an equality condition among the two conducting phases:

$$i_{ONphase\ 1} = i_{ONphase\ 2} \tag{3}$$

This requires only one regulator to be active, which imposes the voltage difference between the two active phases. Its tuning must consider load consisting of twice the impedance. As already mentioned, the third (open-circuit) phase should be still fed with a "probing" voltage, e.g. a sinusoidal signal having amplitude

$$V_{ff} = 2\pi f_{out} L_{out} \cdot \sqrt{2}\, I^*_{RMS} \tag{4}$$

Where I^*_{RMS} is the desired RMS current value. Application of this stimulus allows arc ignition to happen as soon as appropriate conditions are met (i.e. the electrodes are moved such that the distance between the electrode tip and the metallic material becomes sufficiently small), while ensuring limited ignition current at the same time.

It is worth highlighting that each mode transition introduces a transient condition (especially from the control point of view) and thus requires careful management, e.g. regarding initial conditions of integral regulators. In fact, this is crucial for achieving smooth operation (i.e. avoiding overshoot, over-current and partial instability events) and fast recovery after the occurrence of undesired conditions.

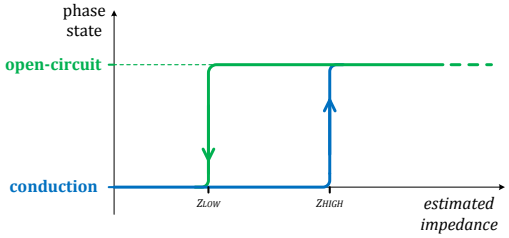

Fig. 2. Open-circuit detection logic.

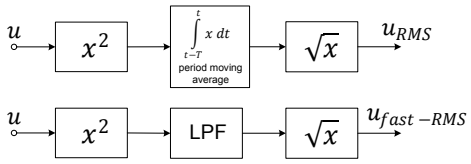

Fig. 3. Normal RMS calculation (top) vs. "fast-RMS" algorithm (bottom).

B. Simple (Scalar) Control

The scalar control mode consists in the generation of three voltage waveforms, phase-shifted by 120 degrees. The amplitude of each is set by the RMS current regulator. The feedback loop compares the measured RMS value of each output current to the reference value, and modifies the voltage magnitude accordingly, as shown in Fig. 4 (for phase a). A feedforward amplitude value

$$V_{ff} = 2\pi f_{out} L_{out} \cdot \sqrt{2}\, i^*_{RMS} \tag{5}$$

is added, with the main purpose of compensating for the expected voltage drop on the known inductance (i.e. the series inductance between the inverter output and the electrode tip). This value also corresponds to the voltage stimulus applied to open-circuit phases, in order to provide a "probing" voltage for the ignition of discharge (electric arc), while ensuring limited short-circuit current (as already introduced in paragraph III.A).

This kind of controller achieves good performance in relatively steady conditions (e.g. final melting stage [5]) and allows to easily manage the open- and short-circuit conditions. However, the control bandwidth is heavily limited by the feedback delay, which is represented by the calculation of the RMS current, acting as a moving-average filter. With the aim of simplifying numerical implementation and reducing the equivalent phase-lag introduced by RMS calculation, a simpler algorithm has been adopted, which exploits a first-order low-pass filter having a reduced time-constant with respect to the length of the moving-average filter (i.e. one fundamental period). The adopted algorithm, which will be designated as "fast-RMS" in the following, is sufficiently accurate (although its output shows higher ripple) and much faster and less memory consuming than the typical implementation.

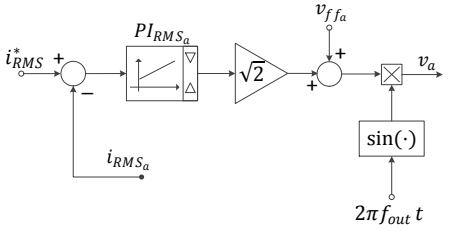

Fig. 4. Scalar current schematic (phase a).

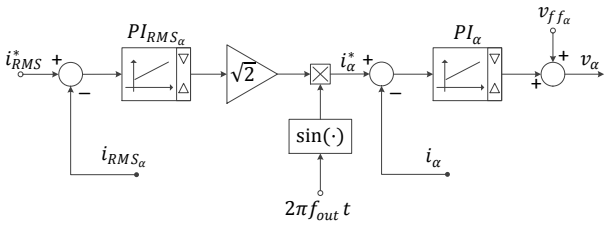

Fig. 5. Vector control loop schematic (α-axis).

C. *Vector control (with impedance estimation-based adaptation)*

In the proposed vector control approach, current regulation is implemented in the stationary-reference frame, by means of two nested control loops (Fig. 5). The outer one (RMS) generates a suitable value for the RMS current reference, which is applied to the real current controller (depicts a simplified schematic for the α-axis). The RMS control loop was introduced to cope with current harmonics (which substantially contributes to the RMS value). Since distortion cannot be eliminated, at least the RMS value (which quantifies the thermal effect) is driven to the desired value. Fig. 5 depicts a simplified schematic for the α-axis, the β-axis one differs only in the phase of the phase of the sine wave for current reference calculation, which is shifted by 90 deg. It is worth noticing that, in this case, the RMS regulator outputs the amplitude of a *current* sine wave, while in the scalar control the regulator output is assigned to the voltage amplitude.

The outer regulation loop has been introduced in order to compensate for the typically large harmonic content of current, which brings non-negligible contribution to the RMS value. In fact, given the low switching frequency and load characteristics (i.e. imbalance, variability, non-linearity), it is not possible to reduce current harmonic distortion to a great extent, as simulations pointed out. In general, the RMS control dynamics will be very slow (i.e. in the order of few Hz) with respect to the real current control loop, for stability reasons and in order to guarantee smooth starting at the beginning of the process or, in general, after changes in the control mode. Tuning of this regulator is relatively simple, since the dynamics of the controlled plant is close to unitary gain and dominated by the fast-RMS calculation low-pass filtering effect. Since the desired bandwidth will be lower than the fast-RMS bandwidth, and much lower than the current control one, a basic way for tuning the RMS loop is to set the proportional gain equal to the desired bandwidth (in rad/s), while the regulator time-constant equal to the fast-RMS one, i.e.

$$K_{p_{RMS}} = \frac{B_{RMS}}{B_{fast\text{-}RMS}} \quad , \quad \tau_{RMS} = \frac{K_{p_{RMS}}}{K_{i_{RMS}}} = \frac{1}{2\pi\, B_{fast\text{-}RMS}} \tag{6}$$

where B_{RMS} is the desired RMS regulation bandwidth (in Hz) and $B_{fast\text{-}RMS}$ is the fast-RMS low-pass filtering bandwidth (in Hz). Lower values of τ_{RMS} will result in higher disturbance rejection, thus faster recovery after changes in load behavior and consequent distortion of the controlled current.

As can be seen in Fig. 5, actual current control is based on sampled current feedback i_α, which is compared to the sinusoidal reference generated based on the RMS regulator output. A feed-forward voltage component is added, which is calculated as for the scalar control in (4), in order to compensate for the expected inductive drop.

Design of the regulator is complicated by the extreme uncertainty on load behavior. In fact, arc behavior can vary widely (in principle, from open- to short-circuit), and normal voltage vs. current characteristic is non-linear. However, the presence of constant and known series inductance and the minimum resistance value (i.e. due to the inverter to electrode connections) allow to make some considerations on stability. If a first-harmonic simplification is considered, simple design rules for the current regulator gains such as the following, based on zero-pole cancellation,

$$K_{p_c} = 2\pi B_c\, L_{out} \quad , \quad \tau_c = \frac{K_{p_c}}{K_{i_c}} = \frac{L_{out}}{R_{nom}} \tag{7}$$

where B_c is the desired current control bandwidth in Hz, R_{nom} is the nominal resistance (i.e. the ratio between nominal arc voltage and current), ensure stability in a wide range of equivalent arc resistance, as shown in Fig. 6 for arc resistance between 0.1 and 10 times the nominal value. Smaller time-constant values lead to better disturbance rejection, but decrease, on the other hand, the stability margin.

In order to achieve a better compromise between stability and performances, a gain adaptation algorithm has been applied, in which the integral gain value is recalculated based on the on-line estimate of impedance:

$$K_{i_{c_{\alpha,\beta}}} = 2\pi B_c\, \hat{Z}_{\alpha,\beta} \tag{8}$$

The estimates $\hat{Z}_\alpha$, $\hat{Z}_\beta$ are calculated based on the ratio between RMS values of $\alpha\beta$ voltage and current, as in (1).

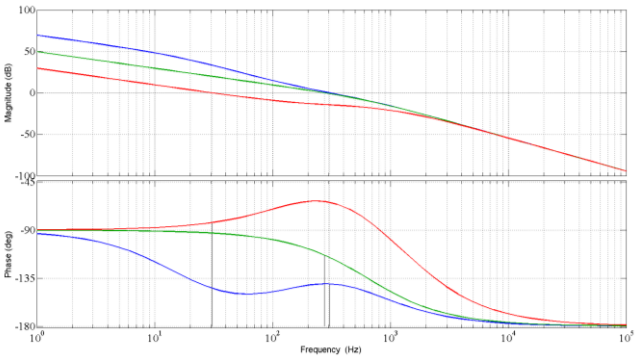

Fig. 6. Bode diagrams of the current control open-loop transfer function designed as in (7), with different load resistance values (green: $R = R_{nom}$, blue: $R = 0.1\, R_{nom}$, red: $R = 10\, R_{nom}$).

D. *Quasi-Zero Latency Current Control*

In order to meet the bandwidth and disturbance rejection requirements, a high-gain and low-latency current control path is required. Given the very low switching frequency, maximum duty-cycle update rate will be very low, although double-update PWM is applied. A single control-cycle delay would theoretically limit the bandwidth to approximately 200 Hz but, due to the variability of the load, the bandwidth would need to be less than 150 Hz.

However, it can be assumed that executing the time-critical part of control algorithm (i.e. the instant current control) would take less than 100 µs in the worst-case (e.g. large communication protocol latency). This means that the actual control delay, i.e. the time elapsed between current sampling and loading of the compare values in the PWM peripheral, can be reduced by at least 5 times (i.e. from 500 to 100 µs). Fig. 7

shows the time diagram of the adopted implementation. It is important to mention that, in this case, sampling is no more synchronous with the PWM, i.e. the sampled current value will no more correspond to the average current within the switching period. Deviating from synchronous sampling [9] required proper current compensation.

In order to overcome this accuracy issue, two different methods have been tested in simulation, both exploiting double current sampling for each PWM period, i.e. both at the beginning of the period and 100 µs before, when the algorithm execution is started. In one case, the sampling accuracy is improved only for the RMS value calculation and regulation (i.e. for the part of the algorithm that is not strictly real-time), which is performed at a different time instant with respect to the instant current control. The second solution introduces current sample compensation, i.e. prediction of the current value which will occur 100 µs after.

The reduction in equivalent delay in the regulation loop is from 1 ms (i.e. the sum of half switching period and one control update period) to 600 µs, i.e. (i.e. one control update period plus 100 µs), allowing a practical increase of the stable control bandwidth from 150 to 300 Hz.

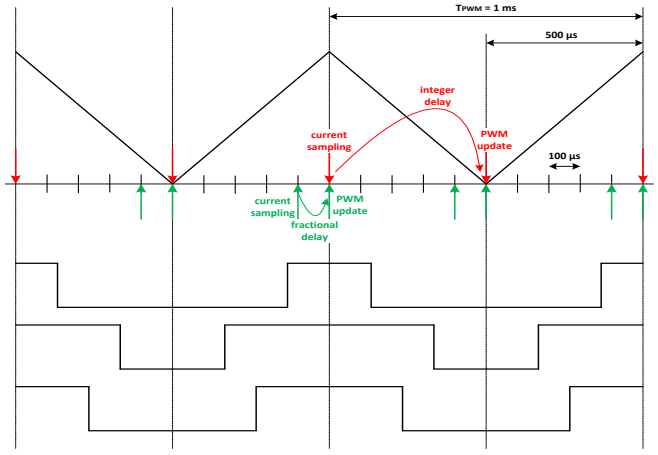

Fig. 7. "Quasi Zero Delay" timing diagram.

E. Control of parallel inverter stages

As already mentioned, the converter stage is composed by two three-phase inverters in parallel, coupled by means of two series inductors (no capacitor is added at the connection node). A peculiar control strategy has been developed in order to deal with the degrees of freedom of the system, which is similar to the method [7], but has some important differences. In fact, if the same voltage references are given to the two modules, possible physical or driving imbalance between the two branches (e.g. due to differences in power components, propagation delay, temperature or other hardware parameters) would result in different currents to be flowing. Moreover, the system could be required to run with different currents, e.g. for energy-saving, for fault-tolerance reasons or due to temperature balancing issues.

This issue has been addressed by adopting a specific control strategy (on top of the normal current control), where regulators based on a novel differential- and common-mode framework transformation have been studied, developed and implemented. The basis of the method will be briefly introduced in the following.

The equivalent circuit for parallel inverter configuration is shown in Fig. 8. Inductances L_1 and L_2 in series with the Voltage Source Inverter equivalent elements (V_1 and V_2) represent equal impedances which separate inverters. The load is represented by a single impedance and an arbitrary voltage generator. Indeed, it will be shown that the behavior of parallel current sharing is not affected by the characteristics of the load, i.e. complete decoupling can be obtained between the dynamics of current imbalance (i.e. $I_1 - I_2$) with respect to common-mode current I.

In the following, Laplace domain representation of the circuit shown in Fig. 8 will be considered. All quantities, including impedances, will represent Laplace transforms and/or transfer functions. The approach is the most general, considering N branches, until the last equations, where the two-parallel case is specifically analyzed. The voltage across the parallel branch can be written using the Millman's theorem:

$$V_{AB} = \frac{\frac{V_1}{Z_1} + \frac{V_2}{Z_2} + \frac{V_{load}}{Z_L}}{\frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_L}} \tag{9}$$

where Z_1 and Z_2 are the impedances of L_1 and L_2, respectively, which will be considered almost equal in the following, i.e. $Z_1 \approx Z_2 = Z_N$ (i.e. small imbalance between inverter coupling inductances is assumed). If the common-mode voltage is defined as

$$V_{AVG} \triangleq \frac{\sum V_x}{N} \tag{10}$$

where, for the case considered here, $x = 1,2$ and $N = 2$. Equation (9) can then be simplified:

$$V_{AB} = \frac{\frac{V_1 + V_2}{Z_N} + \frac{V_{load}}{Z_L}}{\frac{2}{Z_N} + \frac{1}{Z_L}} = \frac{1}{D}\left(\frac{\sum V_x}{Z_N} + \frac{V_{load}}{Z_L}\right) \tag{11}$$

with D being

$$D = \frac{N}{Z_N} + \frac{1}{Z_L} = \frac{NZ_L + Z_N}{Z_N Z_L} \tag{12}$$

Currents on each parallel branch can be calculated as

$$\begin{aligned} I_x = \frac{V_x - V_{AB}}{Z_x} &= \frac{1}{Z_N}\left[V_x - \frac{1}{D}\left(\frac{\sum V_x}{Z_N} + \frac{V_{load}}{Z_L}\right)\right] \\ &= \frac{V_x}{Z_N} - \frac{\sum V_x}{DZ_N{}^2} - \frac{V_{load}}{DZ_N Z_L} \end{aligned} \tag{13}$$

Common-mode current can be obtained by summing the currents on each branch:

$$I_{AVG} \triangleq \frac{\sum I_x}{N} = \frac{\sum V_x}{NZ_N} - \frac{N\sum V_x}{NDZ_N{}^2} - \frac{NV_{load}}{NDZ_N Z_L} \tag{14}$$

which results, after simplification, in

$$I_{AVG} = \frac{V_{AVG} - V_{load}}{NZ_L + Z_N} \tag{15}$$

The differential-mode current is $I_{12} \triangleq (I_1 - I_2)/2$, which can be simply obtained from (13):

$$I_{12} = \frac{I_1 - I_2}{2} = \frac{V_1 - V_2}{2Z_N} = \frac{V_{12}}{Z_N} \tag{16}$$

As can be seen from , differential current only depends on differential voltage $V_{12} \triangleq (V_1 - V_2)/2$, while common-mode current I_{AVG} only depends on common-mode voltage, i.e. the dynamics of the two quantities is fully decoupled and can be separately controlled by operating in a transformed system, in which current and voltage signals are separated into common- and differential-mode components.

This allows to consider a single-branch circuit, when analyzing the behavior of the overall three-phase system. In fact, the same control approach can be adopted for the control of the total (or average) current, despite the one single or multiple branches are present. A dedicated control "module" for the management of a specific parallel configuration can then be added separately. It is worth noticing that these results can be easily generalized for cases where different numbers of parallel branches are present, by simply iterating the process of splitting the branches into two groups and calculating the common- and differential-mode currents. The proposed approach has been tested in simulation, confirming the correctness of the findings.

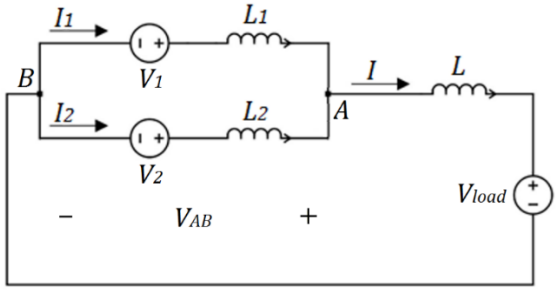

Fig. 8. Equivalent diagram of parallel inverter configuration.

IV. Simulation and Experimental Testing

Simulation of the complete power and control system has been carried out using a dynamical simulation tool. The control algorithm has been implemented in discrete-time, accurately including the effect of real-world delays, which strongly limit regulation performances. The load behavior has been modeled according to different approaches, ranging from a resistor and switch network to an analytical gas discharge model.

A. Arc behavior model

The basic model for the arc behavior consists in stepwise variable resistances in series to each inverter output phase (implemented as a resistor-switch network). This is useful for testing short-circuit, open-circuit, nominal operation and related transitions, but does not reproduce realistic arc behavior, which is characterized by strongly non-linear dynamics. A more refined model has been built based on Cassie-Mayr equations on gas discharge dynamics [1]-[4], which allow to obtain the dynamical value of resistance given the arc parameters and state and accurately representing the arc ignition dynamics. It is worth noticing that previous literature considered sinusoidal voltage input to the arc model, which simplified analysis and simulation, while in this case the aim is simulating current control, which results in distorted voltage and current (i.e. input waveform and amplitude are not known a priori).

Simulation of the arc using the Cassie-Mayr model poses some challenges in the numerical solver and regarding the choice of parameters in order to fit the real behavior. from the point of view of the numerical solution of dynamics equations, issues related to continuity arose during simulation, which required careful implementation. Moreover, most of the model parameters are unknown and it is difficult to relate their values to the resulting voltage vs. current characteristic, so that identification from measurements was not possible.

For these reasons, an empirical model has been developed, which is based on measurements (Fig. 9). The envelope of the voltage waveform was extracted, and recorded voltage has been normalized by dividing the original measured values by the amplitude envelope. This allows to obtain the current vs. normalized voltage scatter plot (blue dots in Fig. 10), which shows an underlying hysteretic behavior. Based on the behavior observed in this diagram, two average curves have been identified, the magenta one for negative-to-positive current and the green one for positive-to-negative current. The voltage resulting from this curve is then multiplied by the measured envelope or by an arbitrary trend of the voltage amplitude. As shown in the lower diagram of Fig. 9, the empirical model fits very well the measured voltage (except for noise).

B. Simulation and experimental results

A comparison of simulation and experimental results in the case of scalar control has been performed. Fig. 11 reports a test sequence (comprising 3ON, 3OFF, 1OFF, SC, in ~60 ms steps), showing current and voltage. The required current setpoint (5 kA peak) is not maintained due to the load impedance variations and overcurrent protection logic is triggered a few times. Experimental measurements from EAF in similar operating conditions is reported in Fig. 12, phase current (green) and electrode voltage (orange). The proposed vector control has also been simulated with the same test sequence, adopting normal sampling and "quasi-zero latency control" (Fig. 13 and Fig. 14, respectively). Standard sampling (Fig. 13) achieves lower distortion than scalar control, but peaking happens during transients and the RMS value does not reach the setpoint. "Quasi-zero latency control" (Fig. 14) achieves the best results (e.g. flat RMS current traces).

It should be noted that the operating conditions considered in simulations concentrate a sequence of transient events in very short times (in order to shorten the total simulation time), which is not likely to happen in the real application. However, acquisitions from the field show that the load is strongly dynamic, especially during the initial phases of the heating. This condition is challenging for the scalar control and vector control with standard sampling approach, while can be effectively managed by the proposed solution with "quasi zero phase-lag".

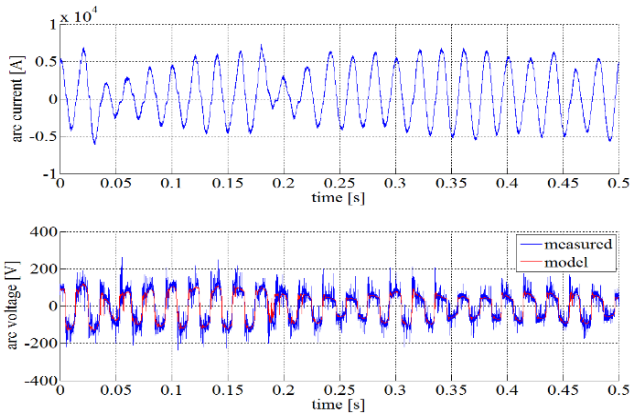

Fig. 9. Measured arc current and voltage.

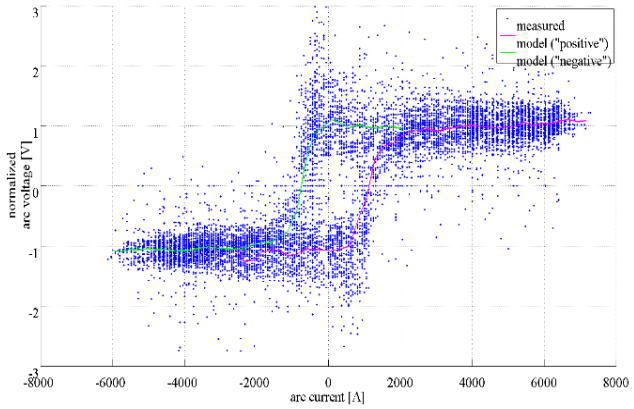

Fig. 10. Voltage vs. current characteristics.

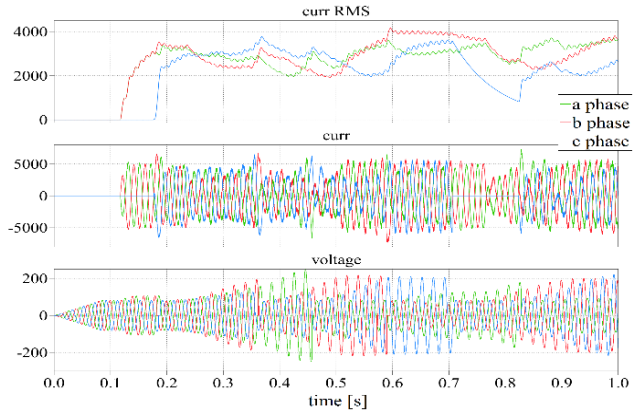

Fig. 11. Scalar control (simulation).

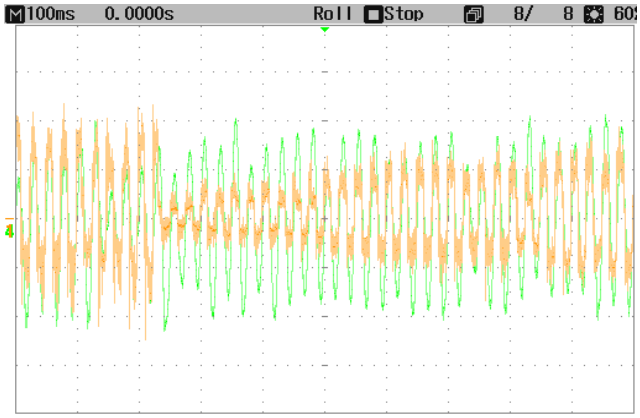

Fig. 12. Scalar control (experimental).

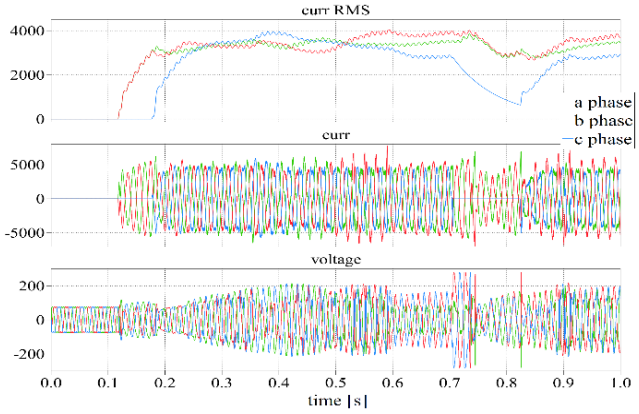

Fig. 13. Standard vector control (simulation)

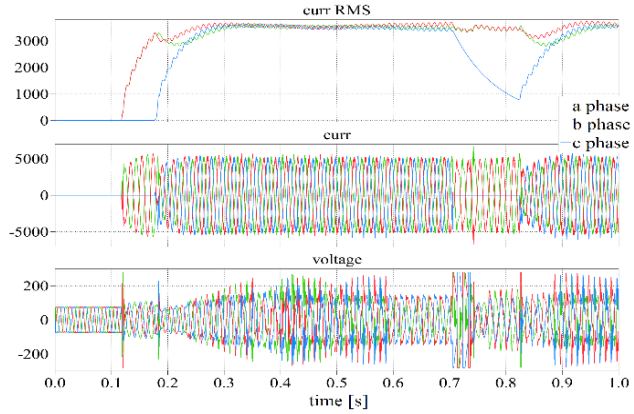

Fig. 14. Quasi-zero latency control (simulation).

TABLE I INVERTER PARAMETERS

Quantity	Value
rated output voltage	80 V_{RMS}
rated output current	10 kA_{RMS}
DC-bus voltage	550 V
switching frequency	1 kHz
number of 3-phase inverter modules	up to 6

V. CONCLUSIONS

In this paper, digital (PWM-based) current control of EAFs by means of three-phase modular inverters has been introduced for the first time. Different issues related to the peculiar characteristics of the arc load (strong non-linearity, variability, imbalance) have been addressed, despite the limitations of the large-power hardware, especially its low switching frequency.

In order to cope with several challenges posed by the application, novel proposals have been presented and validated through simulation:

- scalar control for simple implementation and fast commissioning;
- automatic adaptation of the current controller's integral gain, based on estimated impedance;
- management and control of the different operation modes and related transitions;
- nested control loops for instantaneous current control (inner, faster) and RMS value (outer, slower) and related tuning rules;
- control of paralleled inverters connected through series inductance (without capacitor coupling);
- implementation of analytical (Cassie-Mayr) and empirical model of the arc load dynamical behavior, for simulation of load under PWM-based current control.

The two main solutions proposed, i.e. scalar and vector control in the stationary reference frame have been simulated, including discrete-time effects and inverter PWM. The simpler method, i.e. scalar control, has been tested on an actual plant, showing that it is not able to achieve sufficient arc current stability. Simulation of the vector method demonstrates superior performance, especially when the "quasi zero phase-lag" sampling approach is adopted. The system is able to keep the arc conducting, with properly limited current, even in the case of sudden short-circuit and step increase of arc voltage. The method is expected to improve the exploitation of the plant (increasing the arc on-time) and thus to potentially decrease heating time and energy consumption. Experimental testing of this method is planned for the next future.

REFERENCES

[1] H. Andrei, C. Cepisca, S. Grigorescu, "Power Quality and Electrical Arc Furnaces", *Power Quality Andreas Eberhard, IntechOpen*, April 11th 2011.

[2] K.-J. Tseng, Y. Wang, and D. Mahinda Vilathgamuwa, "An Experimentally Verified Hybrid Cassie–Mayr Electric Arc Model for Power Electronics Simulations," *IEEE Transactions on Power Electronics*, Vol. 12, No. 3, May 1997.

[3] Mahmood Moghadasian, Emad Al-Nasser, "Modelling and Control of Electrode System for an Electric Arc Furnace", *2nd International Conference on Research in Science, Engineering and Technology (ICRSET'2014)*, March 21-2, 2014 Dubai (UAE), pp. 129-133.

[4] J. L. Guardado, S. G. Maximov, E. Melgoza, J. L. Naredo, and P. Moreno, "An Improved Arc Model Before Current Zero Based on the Combined Mayr and Cassie Arc Models," *IEEE Transactions on Power Delivery*, Vol. 20, No. 1, January 2005.

[5] I.A. Pires, M.M.G. Cardoso, B.J.C. Filho, "An Active Series Reactor for an Electric Arc Furnace," *IEEE Industry Applications Magazine*, pp. 53-62, Sept./Oct. 2016.

[6] F. Blaabjerg, "Control of Power Electronic Converters and Systems, Volume 1", Academic Press, 2018.

[7] H. S. Jung, J. M. Yoo, S. K. Sul, H. J. Lee and C. Hong, "Parallel Operation of Inverters With Isolated DC Link for Minimizing Sharing Inductor," in *IEEE Transactions on Industry Applications*, vol. 53, no. 5, pp. 4450-4459, Sept.-Oct. 2017.

[8] D. Siemaszko, "Positive and negative sequence control for power converters under weak unbalanced networks," *2012 Electrical Systems for Aircraft, Railway and Ship Propulsion*, Bologna, 2012, pp. 1-6.

[9] T. Matsui, T. Okuyama, J. Takahashi, T. Sukegawa and K. Kamiyama, "A high accuracy current component detection method for fully digital, vector-controlled PWM VSI-fed AC drives," *Power Electronics Specialists Conference, 1988. PESC '88 Record., 19th Annual IEEE*, Kyoto, Japan, 1988, pp. 877-884 vol.2. doi: 10.1109/PESC.1988.18220.